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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/800,213	03/06/2001	John Howard Coleman		4985

7590 06/08/2006

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EXAMINER	
TRAN, MINH LOAN	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

A

Office Action Summary	Application No.	Applicant(s)	
	09/800,213	COLEMAN, JOHN HOWARD	
	Examiner	Art Unit	
	Minh-Loan T. Tran	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on 08/10/2005. These drawings are acceptable.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5-11, 13 are rejected under 35 U.S.C. 103(a) as being obvious over Jianming Li et al. (Properties of Silicon-on-defect-layer material, Material Research Society, Vol. 396, pages 745-750, 1995).

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the

application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

With regard to claims 1 and 7, pages 746 and 747 of Li et al. discloses a method for making a semiconductor device having a p-type region, comprising the steps of :
(i) forming an initial region to an initial depth from at least a portion of an initial surface of a semiconductor substrate which has n-type conductivity and an original bulk spreading resistivity (40 Ω-cm);
(ii) heating the initial region, therein to develop an initial spreading resistivity profile having a peak, with peak value greater than the bulk spreading resistivity (see figure 1 of Li et al.)

Li et al. does not disclose the step of removing material from the initial surface portion thereby forming the device region having a new surface from which the resistivity peak is at a reduced depth. However, it would have been obvious to one of ordinary skill in the art to remove the initial surface portion of Li et al. so that the device region having a new surface from which the resistivity peak is at a reduced depth, because such process step is a standard procedure for thinning the semiconductor wafer in order to form the semiconductor devices. Note page 852, right column, lines 12 and 13 of Grisolia et al. (A transmission electron microscopy quantitative study of the growth kinetics of H platelets in Si; Applied Physics Letters, Vol. 76, No. 7, Feb 2000) disclose that removing a surface of a wafer using mechanical thinning and ion beam

milling is a standard procedure for thinning the semiconductor wafer after the proton is implanted and annealed, is cited to support for the well known position. Further, there is no evidence indicating the thickness of the top surface region is critical and it has been held that it is not inventive to discover the optimum or workable range of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicants must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

With regard to claims 2 and 3, Li et al. discloses step (i) comprises implanting particles, wherein the particles are hydrogen ions (page 746.)

With regard to claim 5, page 746 (Experiment) of Li et al. discloses the substrate has n-type conductivity and wherein in step (ii), heating (i.e. annealing at 1180°C for 20 minutes) results in a change of conductivity to p-type in the initial n-type region.

With regard to claim 6 and 13, page 746 (Experiment) of Li et al. discloses the heating (i.e. annealing at 1180°C for 20 minutes) for changing the n-type conductivity type to p-type conductivity type is distinct from heating (i.e. annealing at 900°C for 10 seconds) to develop the initial spreading resistivity profile.

With regard to claims 8-10, the Abstract and pages 746, 749 of Li et al. disclose that the SODL (Silicon-on-Defect-Layer) material is suitable for forming CMOS device in the p-type region.

With regard to claim 11, the Abstract of Li et al. discloses a trench between NMOS and PMOS having a depth of at least to the depth of the peak of the spreading resistivity of the device region, because Li et al. states that the p-n junction in SODL material functions as an isolation of a well in a CMOS device.

Claim 4 is are rejected under 35 U.S.C. 103(a) as being obvious over Jianming Li et al. (Properties of Silicon-on-defect-layer material, Material Research Society, Vol. 396, pages 745-750, 1995) in view of Li et al. (Properties of proton-implanted p-type Si : supports for the models explaning a novel p-n junction in Si, Nuclear Instruments and Methods in Physics Research B 160, pages 190-193, 2000.)

Li et al. (Material Research Society, 1995) does not disclose the substrate has p-type conductivity. However, Li et al. (Nuclear Instruments and Methods in Physics Research B 160, pages 190-193, 2000) discloses proton implanted and annealed p-type Si substrate. Therefore, it would have been obvious to one of ordinary skill in the art to replace the n-type substrate of Li et al. (Material Research Society, 1995) by the p-type substrate of Li et al. (Nuclear Instruments and Methods in Physics Research B 160, pages 190-193, 2000) in order to form the p-n junction in silicon wafer.

Claim 12 is rejected under 35 U.S.C. 103(a) as being obvious over Jianming Li et al. (Properties of Silicon-on-defect-layer material, Material Research Society, Vol. 396, pages 745-750, 1995) in view of Li (5,633,174.)

Li et al. does not disclose a step of growing a crystalline region on the p-type device region. However, Li discloses growing a single crystal silicon on the p-type device region. Note lines 64-67 in column 3 and lines 1-13 in column 4 of Li. Therefore, it would have been obvious to one of ordinary skill in the art to grow the crystalline region on the p-type device region of Li et al. such as taught by Li in order to form a CMOS device having high electron mobility.

Response to Arguments

3. Applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection. This action is not made final.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh-Loan T. Tran whose telephone number is (571) 272-1922. The examiner can normally be reached on Monday-Friday 9:00 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mlt
05/2006

Minh-Loan T. Tran
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Art Unit 2826